Design Challenges With New Bus Technologies

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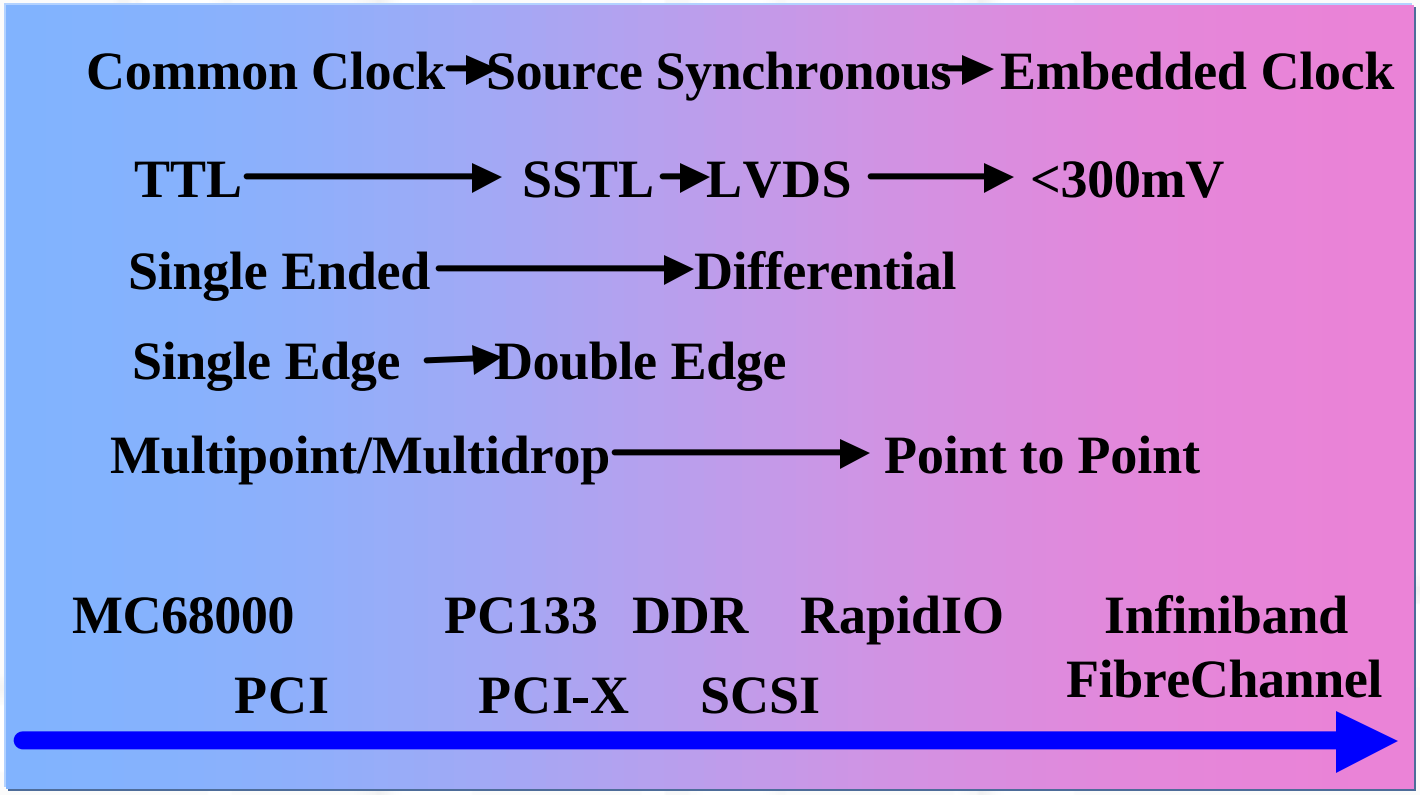
Agenda

- Technology Trends and Challenges
- DDR Overview
- Logic Analysis Challenges in Supporting DDR
- FuturePlus / Agilent DDR Solution

Bus Technology Trends



Bus Technology Challenges: Finding and Maintaining the Data Eye

- Managing jitter budget
  - Crosstalk
  - Intersymbol Interference
  - Clock **AND** Data Jitter
- Managing signal integrity
  - Termination
  - Stubs
  - Signal Loss (Dielectric, Loading)

Bus Technology Challenges: Additional Challenges

- Dealing with multiple strobes
- Clock recovery
- Difficult PCB Layout
- Training algorithms
- Switched Fabric Interconnect

Sources of Jitter on High Speed (DDR) Busses

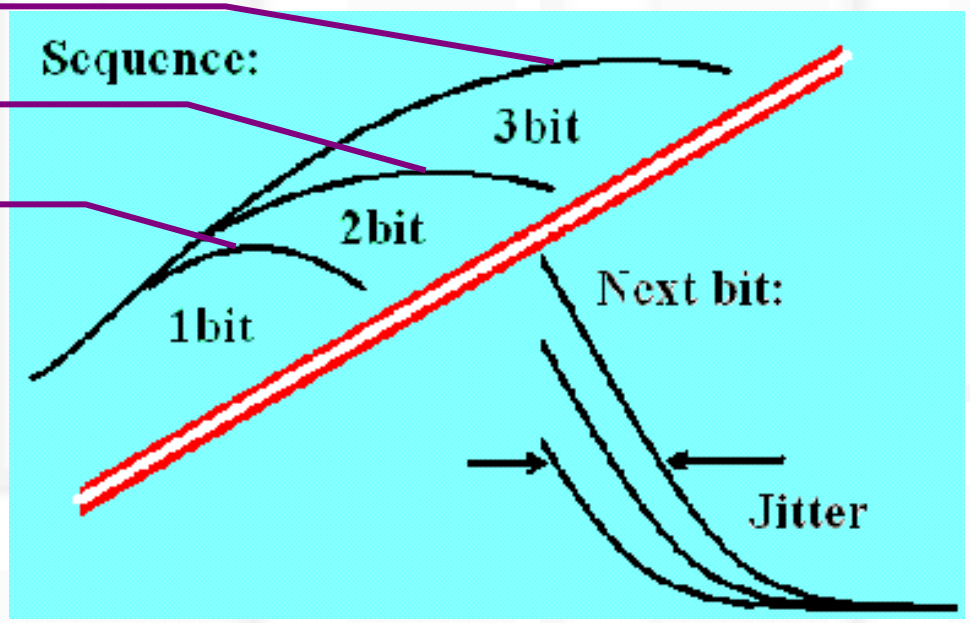
Intersymbol Interference

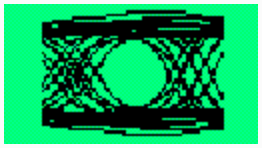
Bit pattern

"01110"

"0110"

"010"

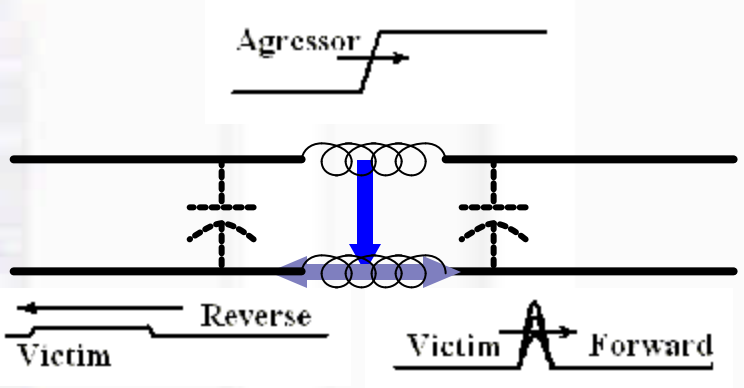


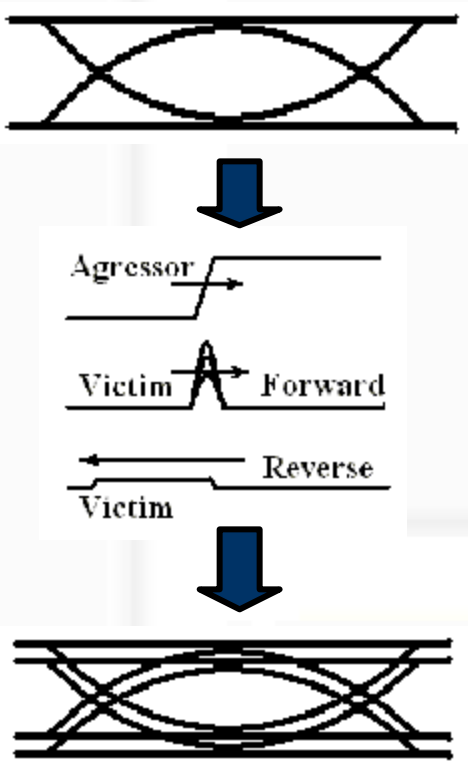


Eye Diagram

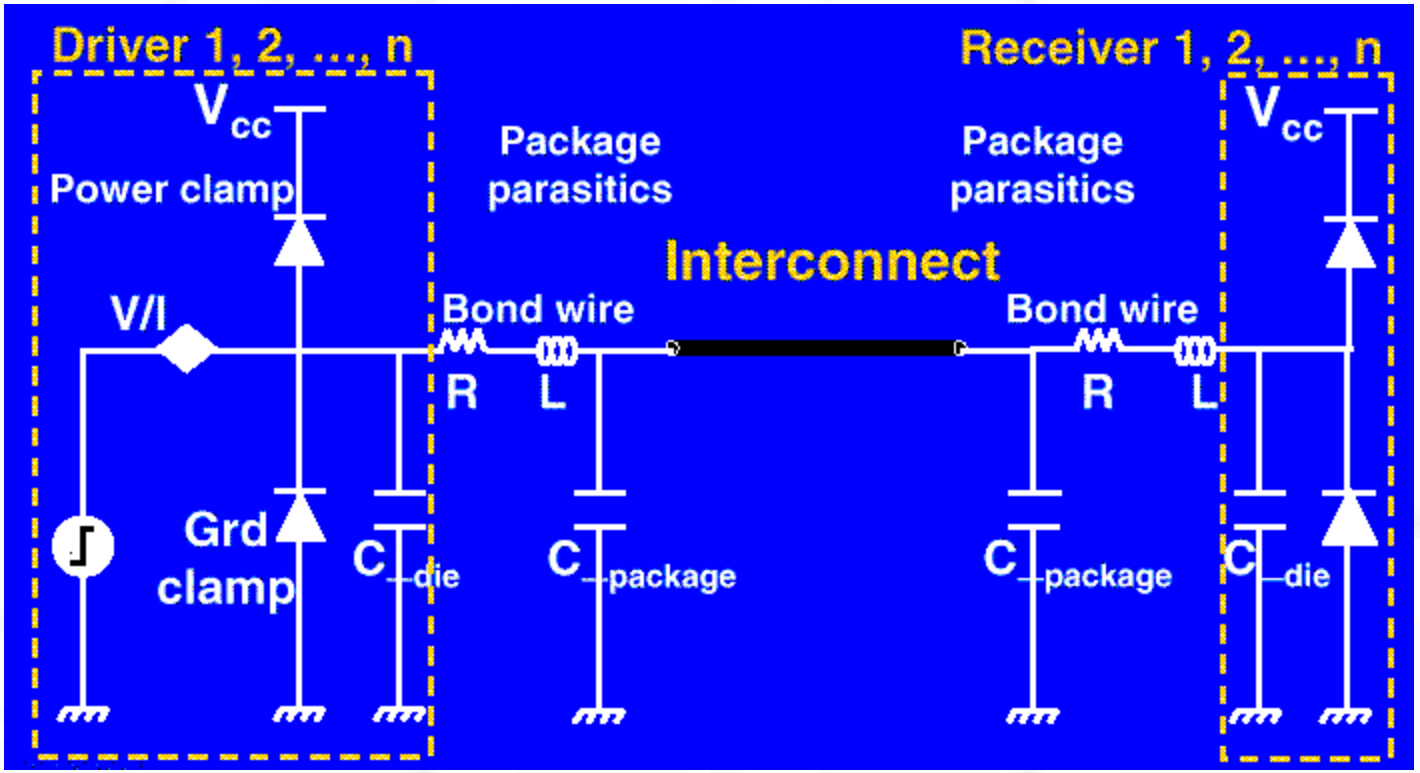
Sources of Jitter on High Speed (DDR) Busses

Crosstalk



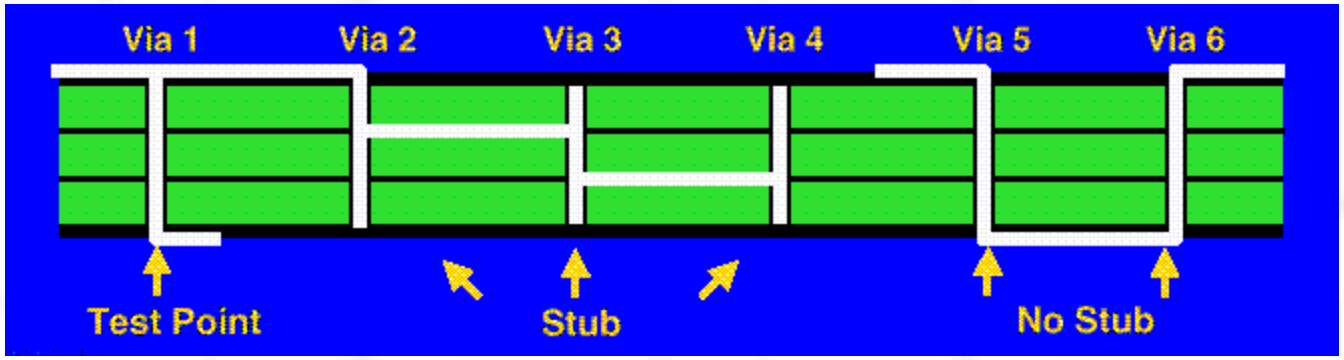


Managing Signal Integrity - Spice Simulation



Unfortunately, It's Only Going To Get Worse

Example: Above 1000Mhz vias can become stubs!

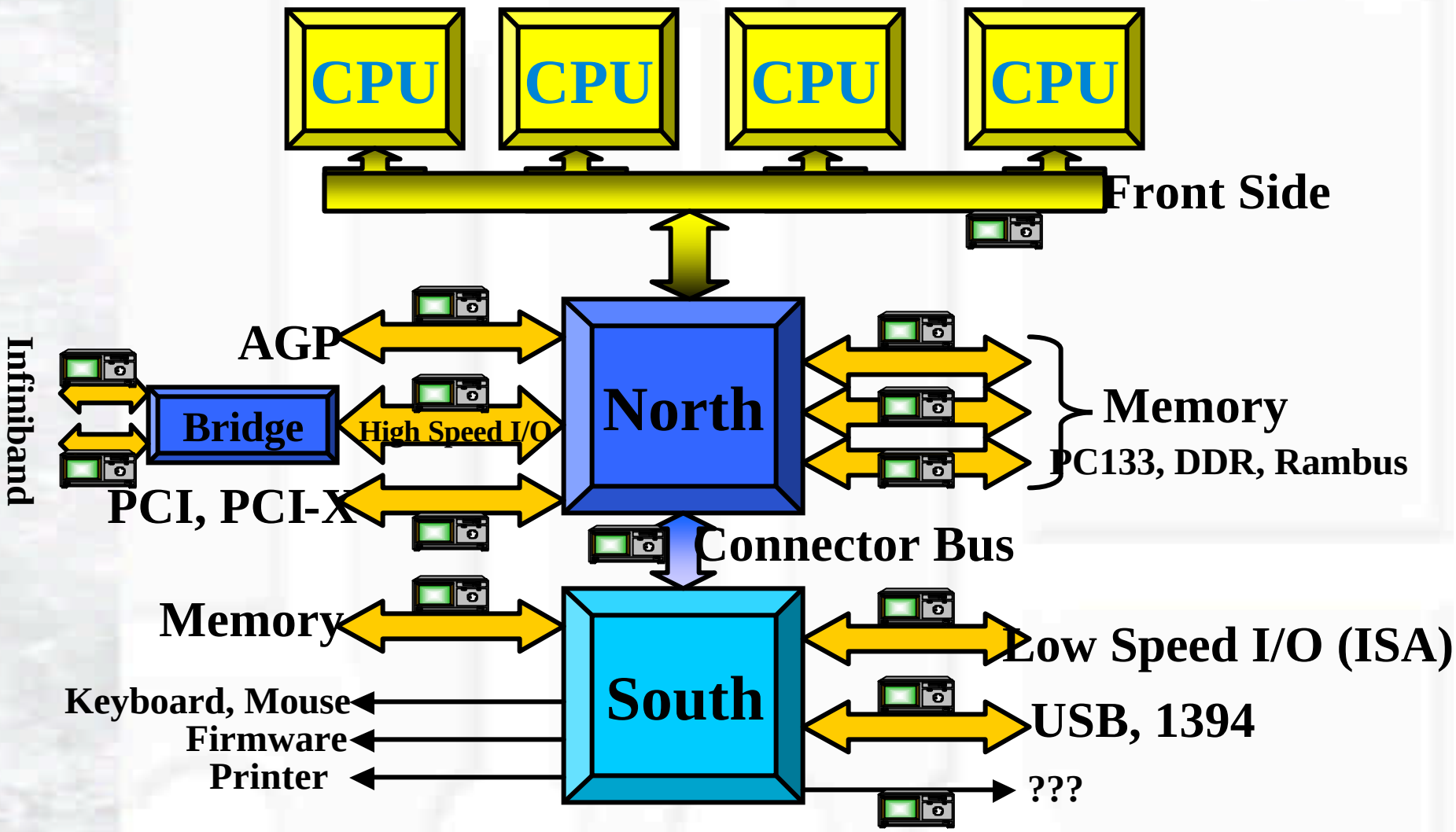


Trends and Challenges: Conclusion

- Higher performance demands are driving a major change in the way busses must be designed and verified.
- System design teams will have to adopt new tools and techniques.

DDR Overview

System Verification



DDR Overview

- DDR has two main parts
  - Command Bus
  - Data Bus

DDR differs from SDR

- Double Data Rate / 2n-prefetch architecture
- Strobe based data bus
- Specific timing and critical specifications for READ and WRITE

PC133 Compared to Double Data Rate DRAM

	PC133	DDR
Speed	100/133 Mhz	200/266Mhz+
#Clocks	1	Up to 19
Eye Size	2V x 4ns	700mv x 1.5ns
Clock Edges	Single	Double
Clock Method	Common	Source Synchronous
Interconnect	Multipoint	Multipoint
Timing	Centered	Centered / Straddle

Rambus -> Double Data Rate DRAM

	Rambus	DDR
Speed	400 Mhz 800MT/s	200/266Mhz+
#Clocks	2 Differential	Up to 19 Differential
Eye Size	400mv x 400ps	700mv x 1.5ns
Clock Edges	Double Pumped	Double Pumped
Data Rate	1.6GB/s	2.1GB/s
Interconnect	RIMMs or continuity modules required all slots	DIMMs Empty slots ok

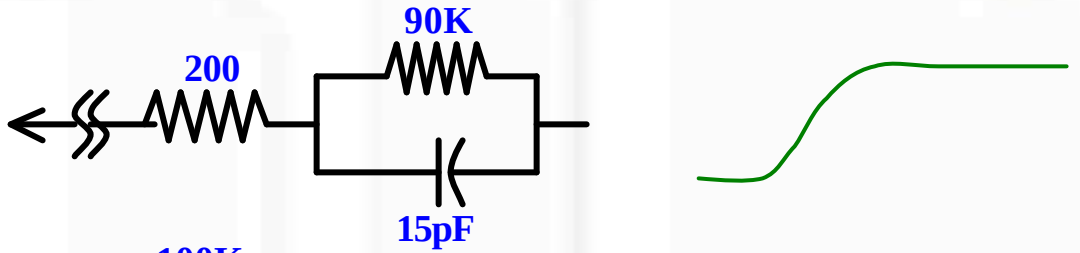
Logic Analysis Challenges in Supporting DDR

DDR Validation - Challenges for Logic Analysis

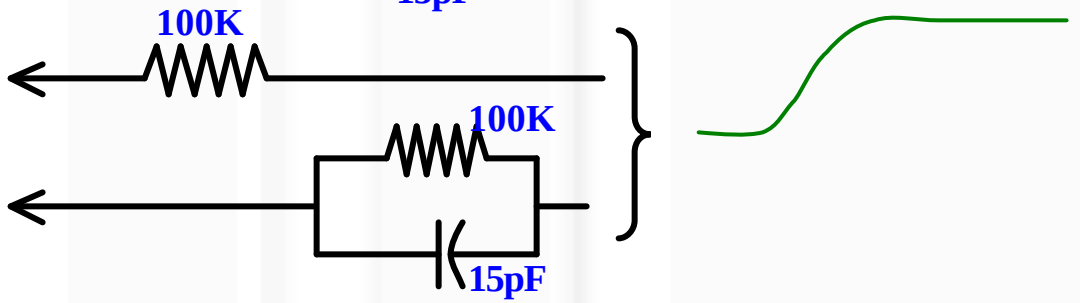
	DDR	Analysis Challenge
Speed	200/266+ Mhz	Triggering, Probing
#Clocks	Up to 19	Clock Selection
Eye Size	700mv x 1.5ns	Data Sampling
Clock Edges	Double	CK
Clock Method	Source Synchronous	Clock recovery
Interconnect	Multipoint	CK
Timing	Centered / Straddle	Clock Generation

Probing at DDR Frequencies

Input Circuit

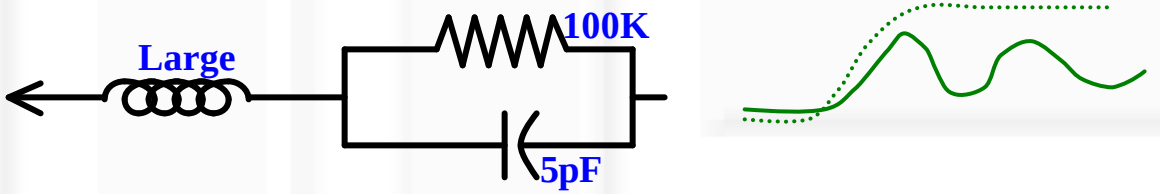


@ 10-20 MHz



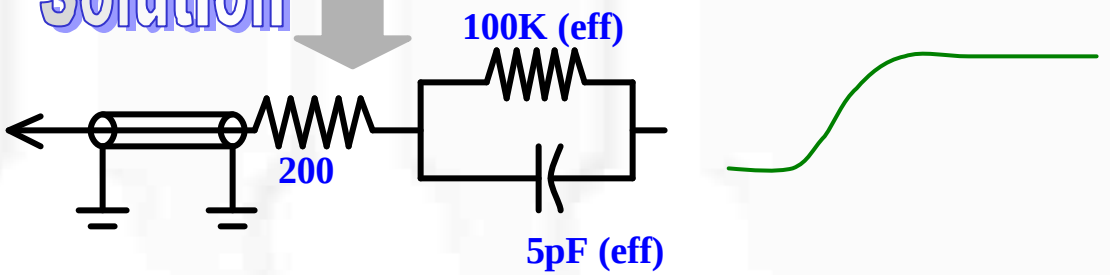
@ 20-50 MHz

@ >50 MHz

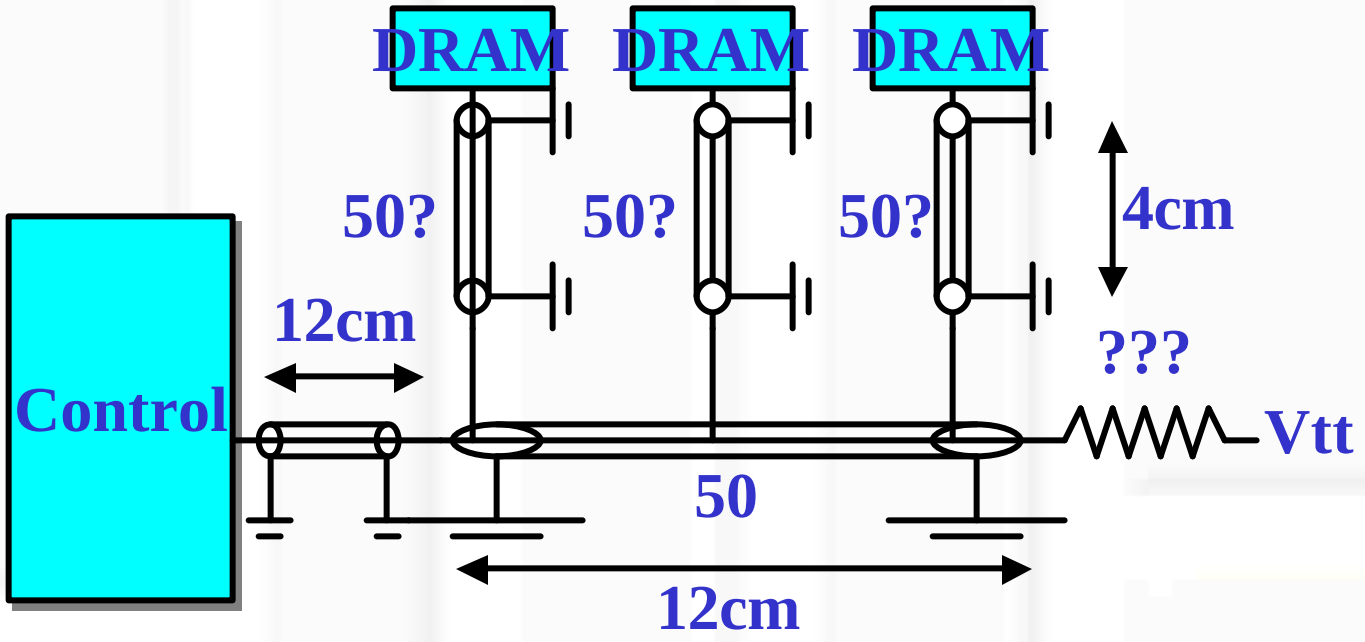


Solution

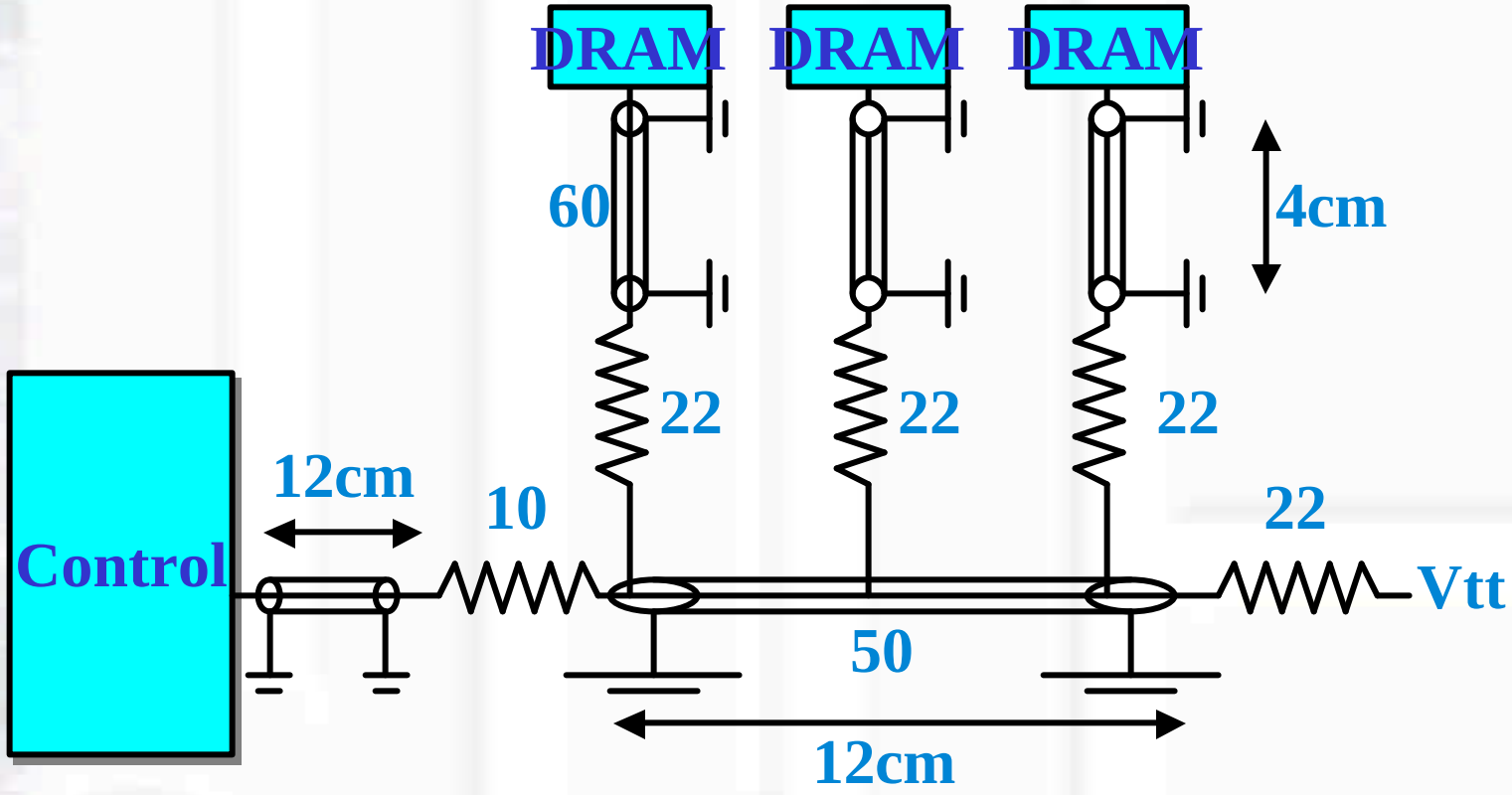
@ 266+ MHz



Signal Integrity Dealing with Stubs



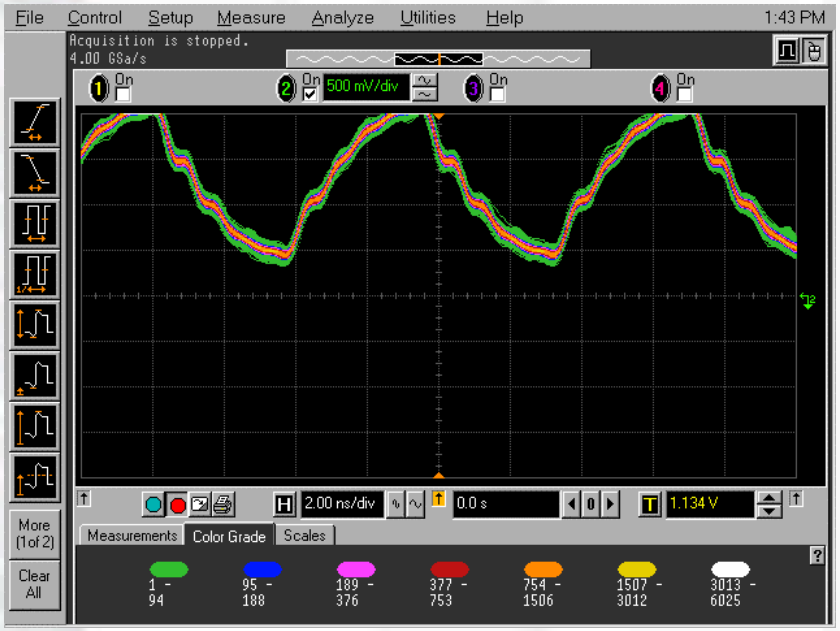
DDR Source Synchronous Bus - Where to Terminate?



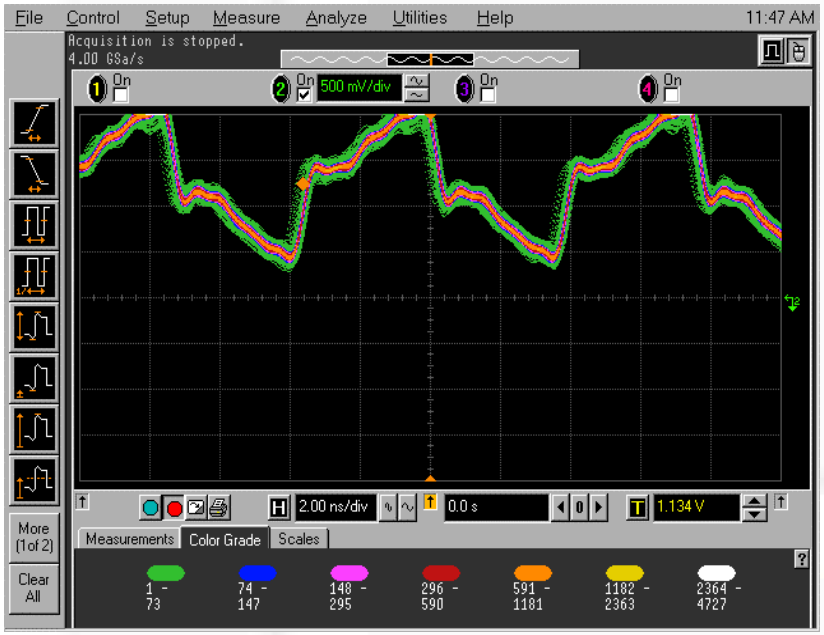
(Answer: Everywhere!)

DDR Signal Integrity: The Margin for Error is Small

DQ51 Write Near Controller At Far End of Bus



b0wrss0192



b3wrss0192

DDR Data Sample Window

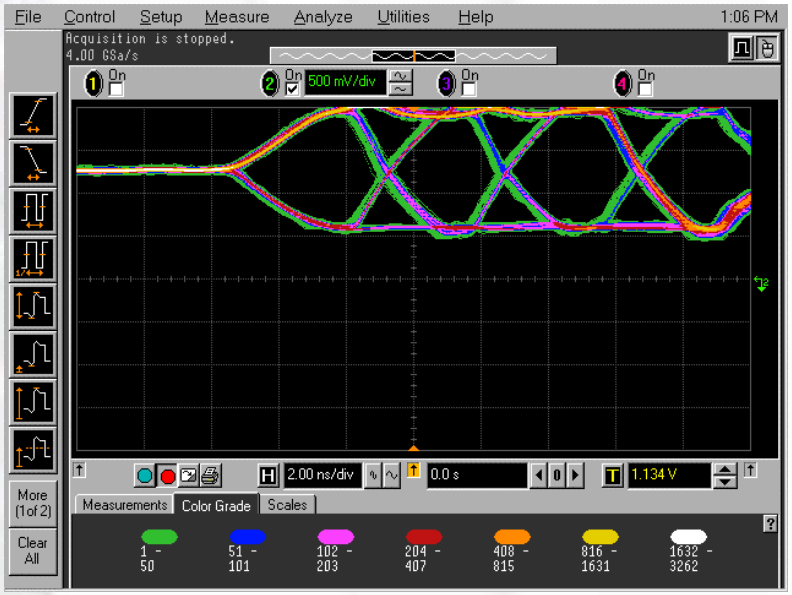
1.5nS

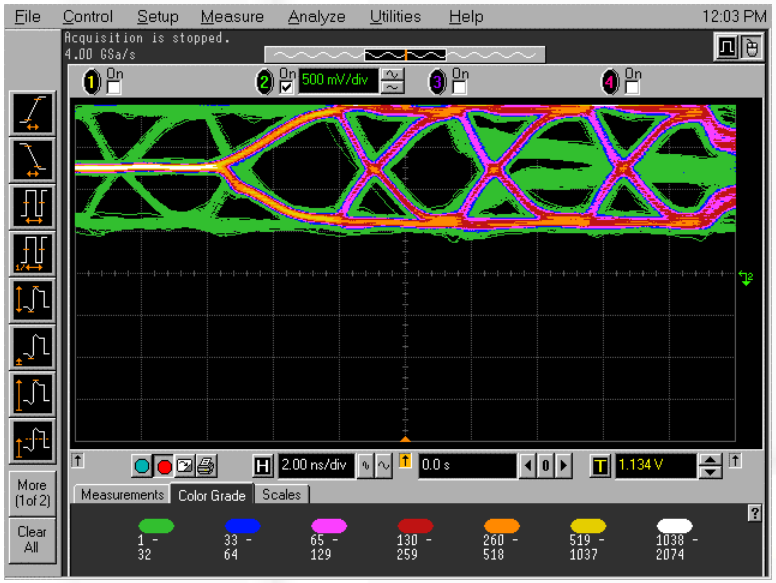
700m

V

Signal Integrity is Important - Especially for Reads

DQ51 Read Near Controller At Far End of Bus

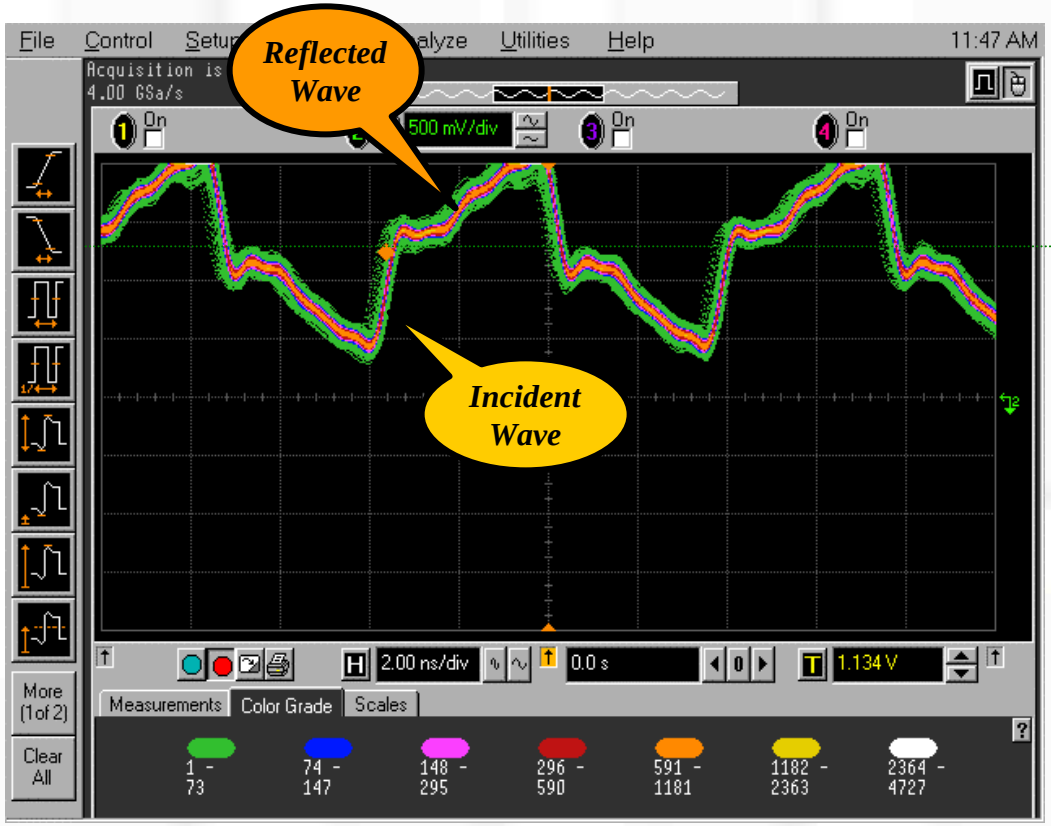




(also write at end of bus)

B3wrss0192

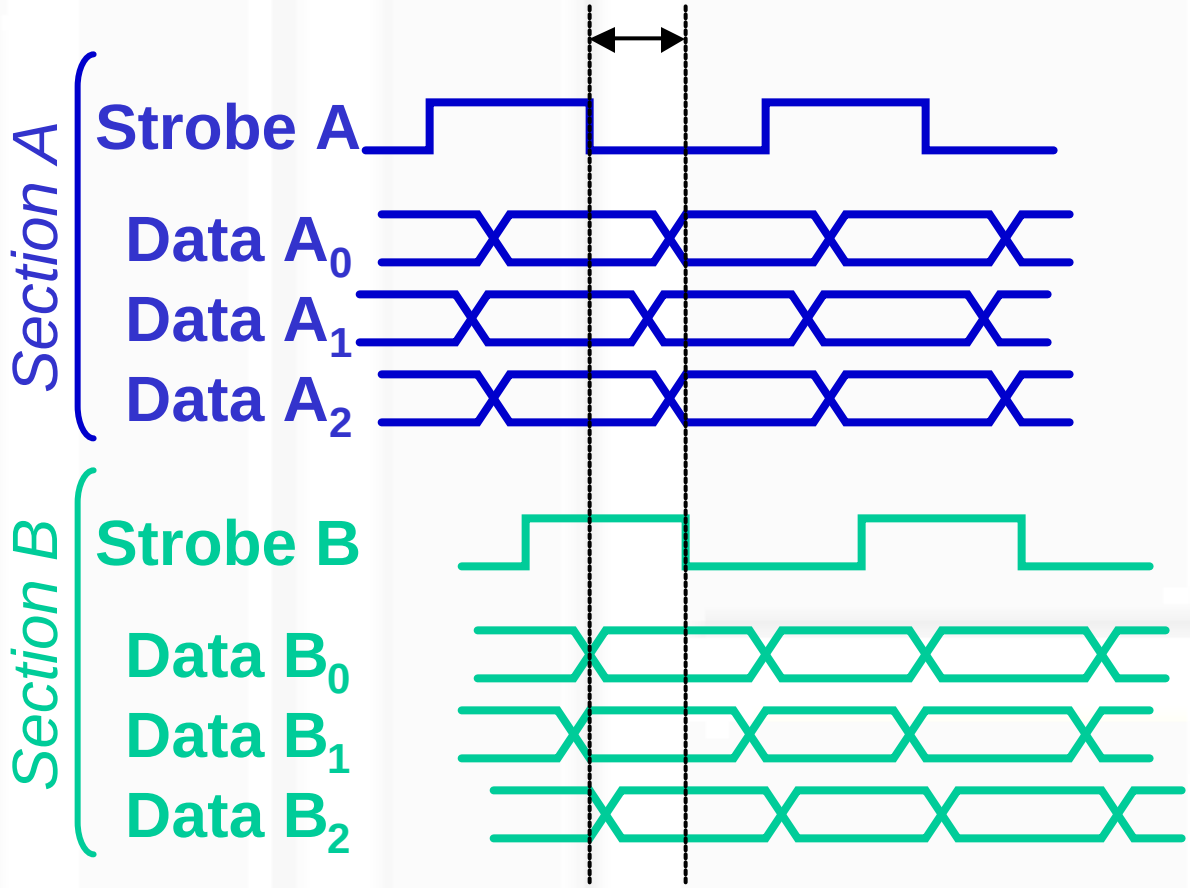
DDR Clock Generation: Where is the real clock edge?



Logic Analyzer Sampling - Which Clock to Use?

- Logic Analyzers cannot sample using 19 clocks - only one can be chosen
- Skews between Sections may be large

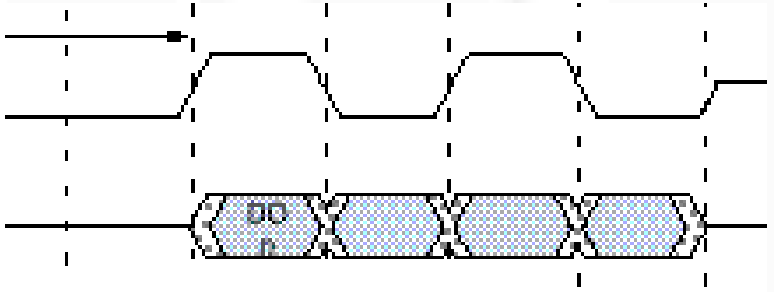
> Traditional solution requires an active probe



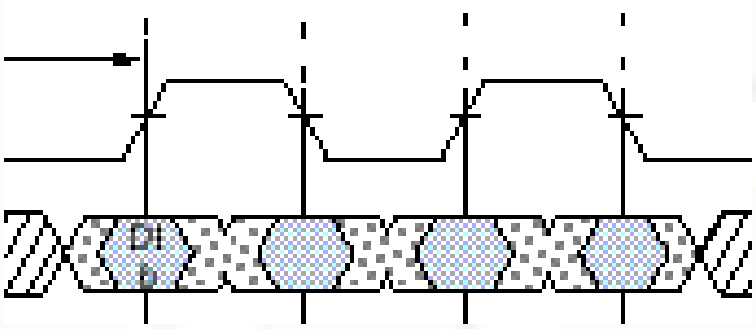
DDR Burst Timing Read or Write?

- Clock straddles data
- Clock centered on data

Read

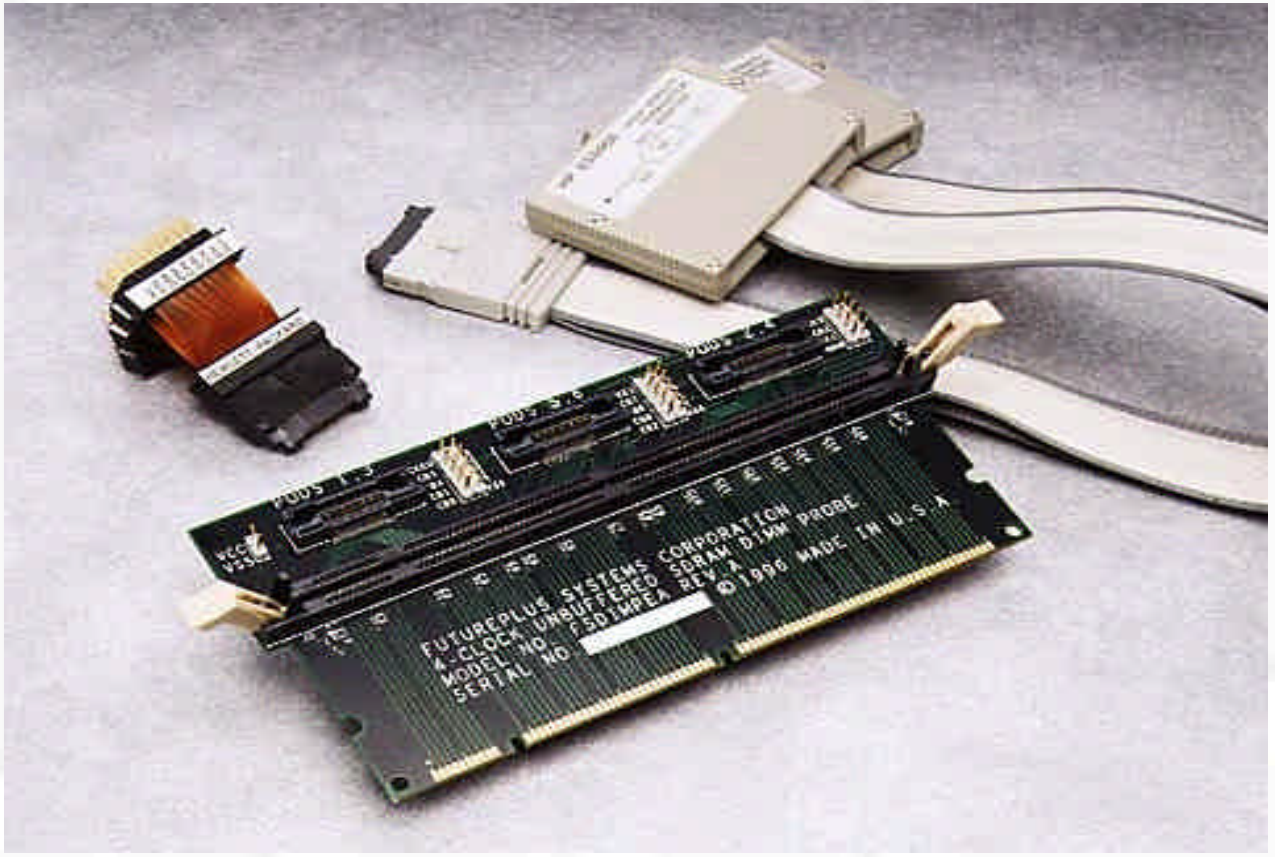


Write



FuturePlus / Agilent DDR Probe

66MHz DIMM Solution



Increasing clock rates and shrinking data valid windows demand advanced solutions. This form factor could prove unreliable for DDR (200MHz and higher) solutions.

Analysis Probe Design: Active or Passive?

- Active Probe
  - + Easy Triggering
  - + Easy Set-up
  - + Higher Speeds / Smaller aperture
  - -- Cost
  - -- Time-to-market
  - -- Size / Heat load
  - -- More LA channels required
  - -- No parametrics

- Passive Probe
  - + Parametric measurements
  - + Low cost
  - + Early availability
  - + Size / Heat load
  - + Flexibility
  - -- Larger data valid window
  - -- Trigger setup more complex
  - -- Calibration required

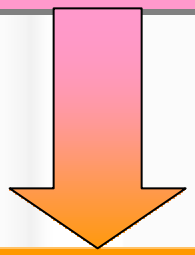
Ideal DDR Solution

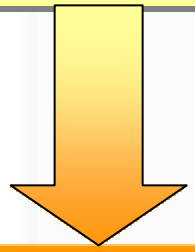
Active Benefits

+ Easy Triggering
+ Easy Set-up
+ Higher Speeds / Smaller aperture

Passive Benefits

+ Parametric measurements
+ Low cost
+ Early availability
+ Size / Heat load
+ Flexibility





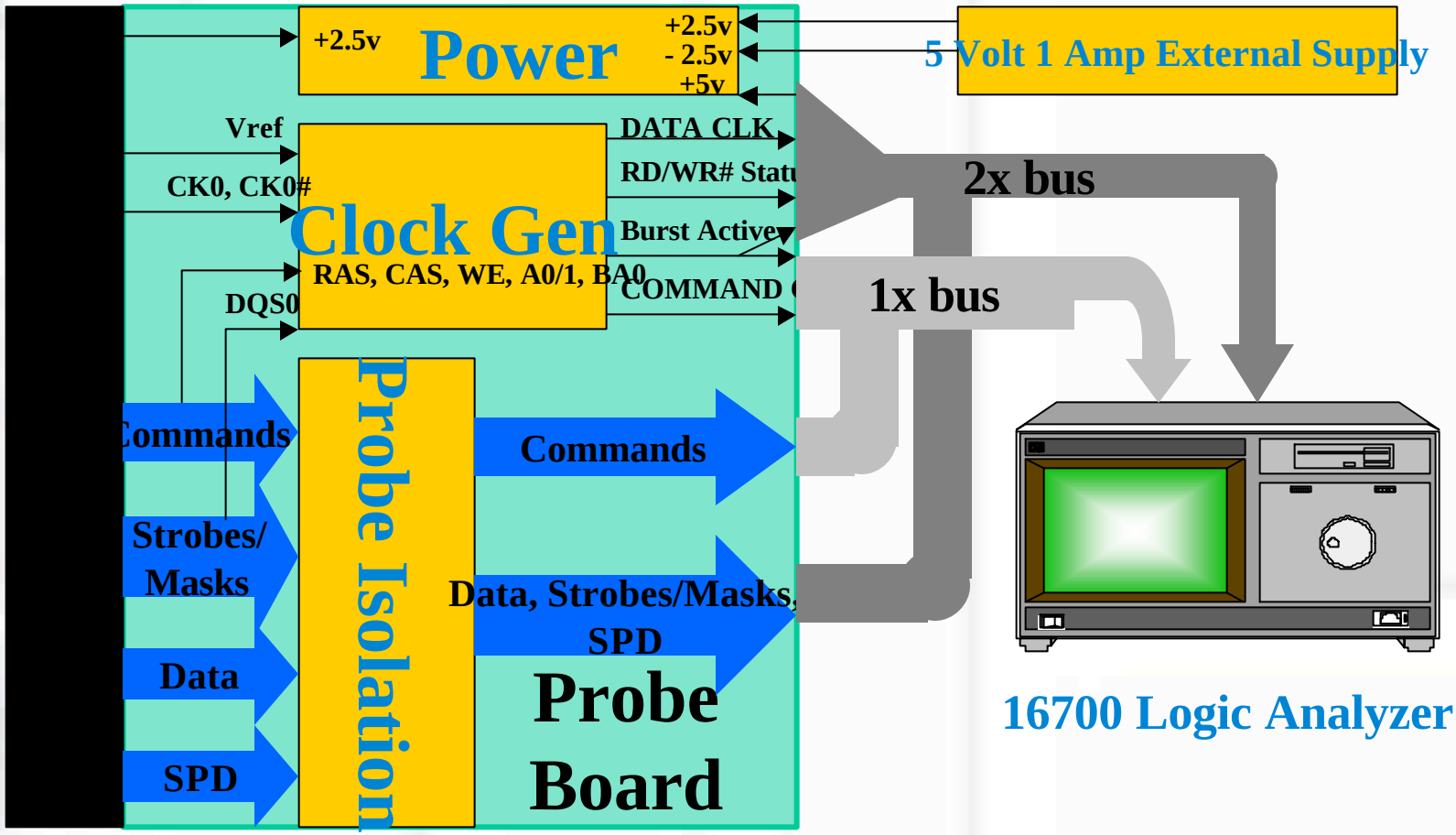
Passive Probe with State Clock Generation

FuturePlus 266MHz DDR Probe

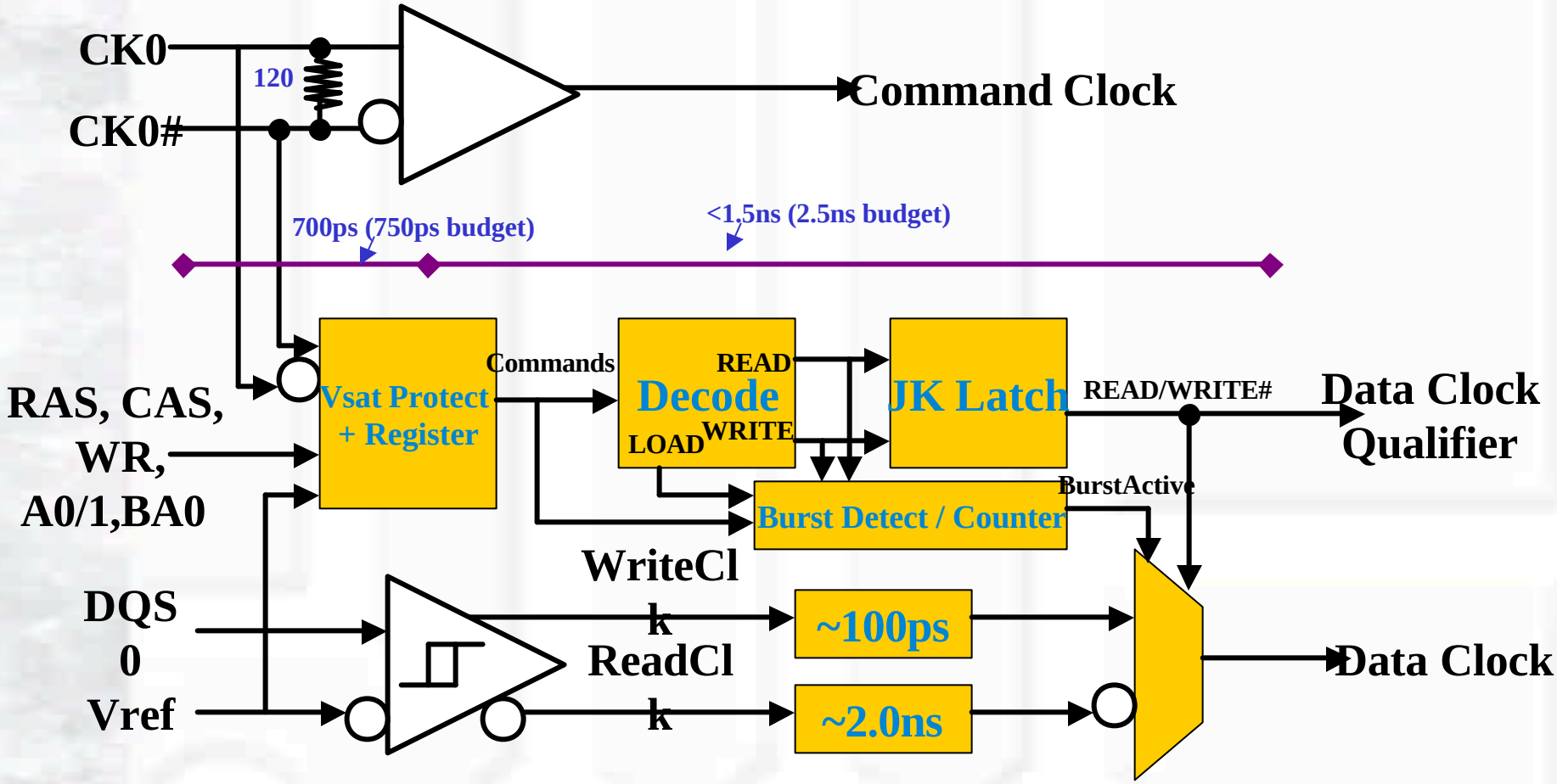
FS 2330

An advanced and elegant solution, supporting timing and state analysis.

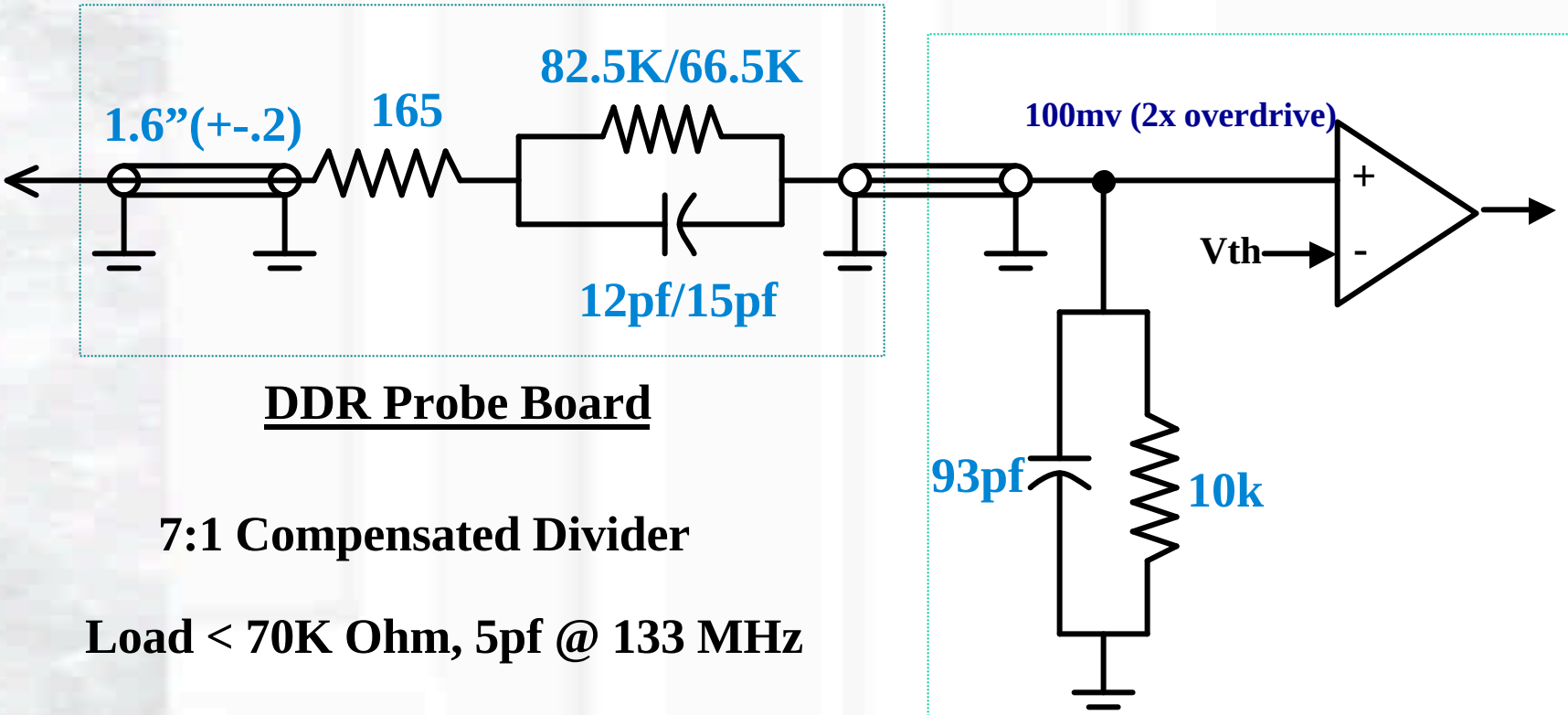
FS2330 Passive DDR Probe



Clock Generator



Passive Probing Network



DDR Probe Board

Logic Analyzer Board

7:1 Compensated Divider

Load < 70K Ohm, 5pf @ 133 MHz

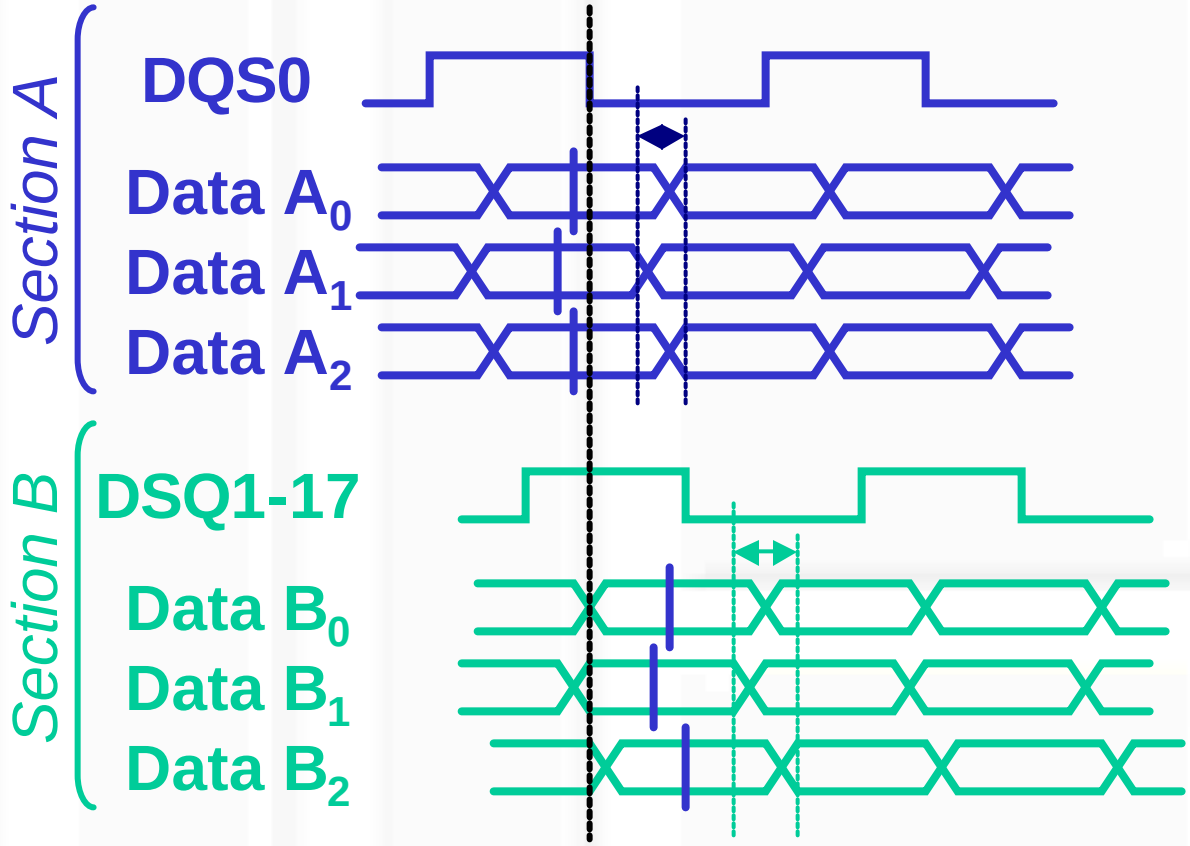
10:1 Compensated Divider

Load < 100K Ohm, 4pf @ 133 MHz

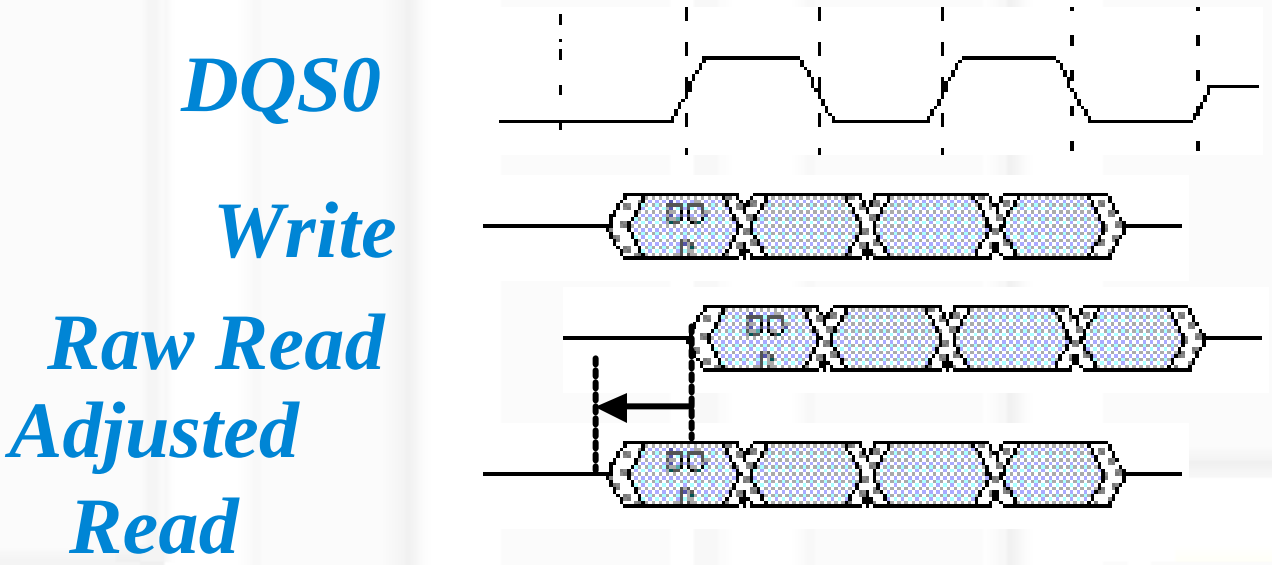
DDR Probe Source Synchronous Data Sampling

- DQS0 samples all data
- Skews between Sections compensated for on each channel

> Logic Analyzer is now able to support state analysis on source synchronous busses with a PASSIVE probe

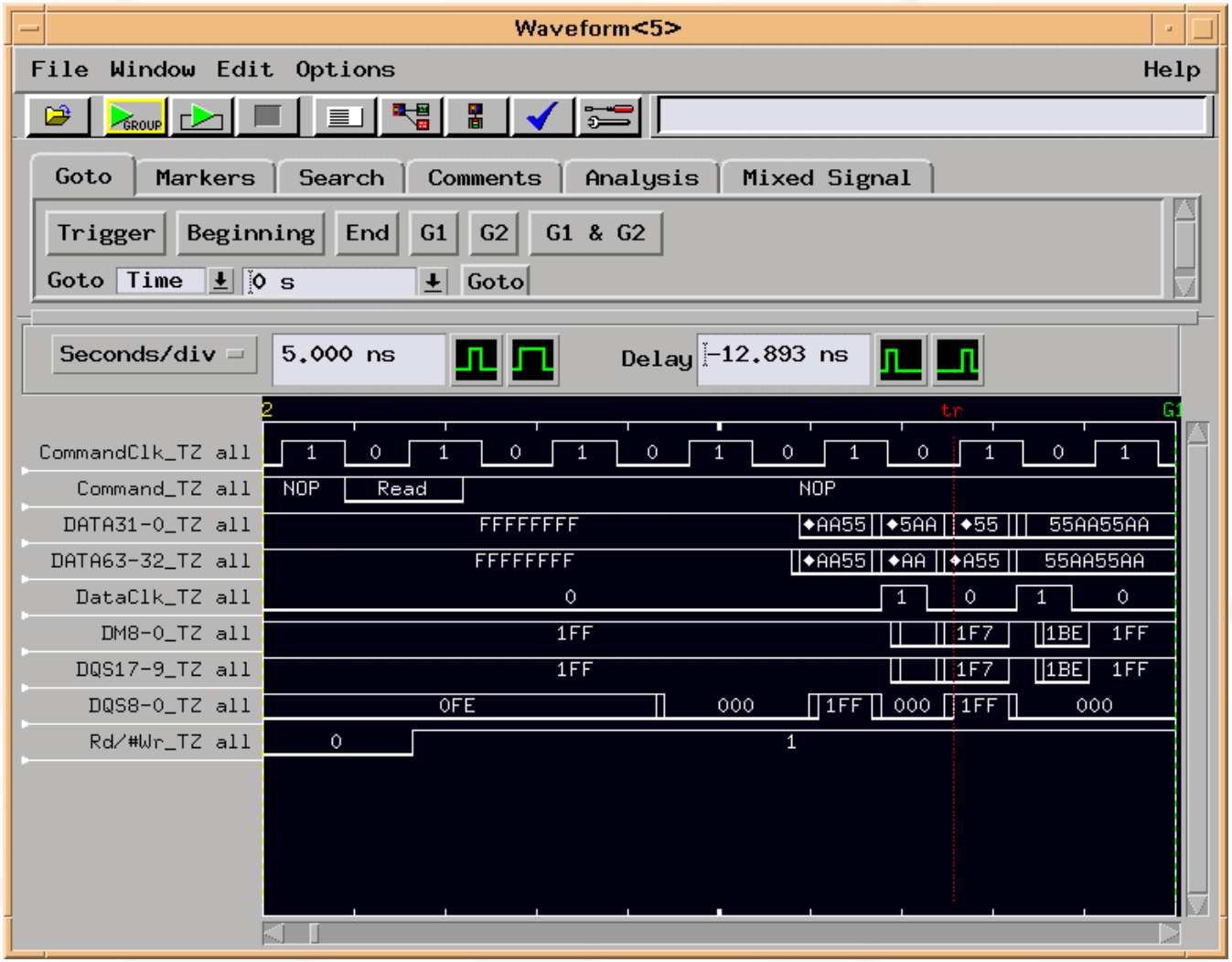


Dealing with Reads AND Writes

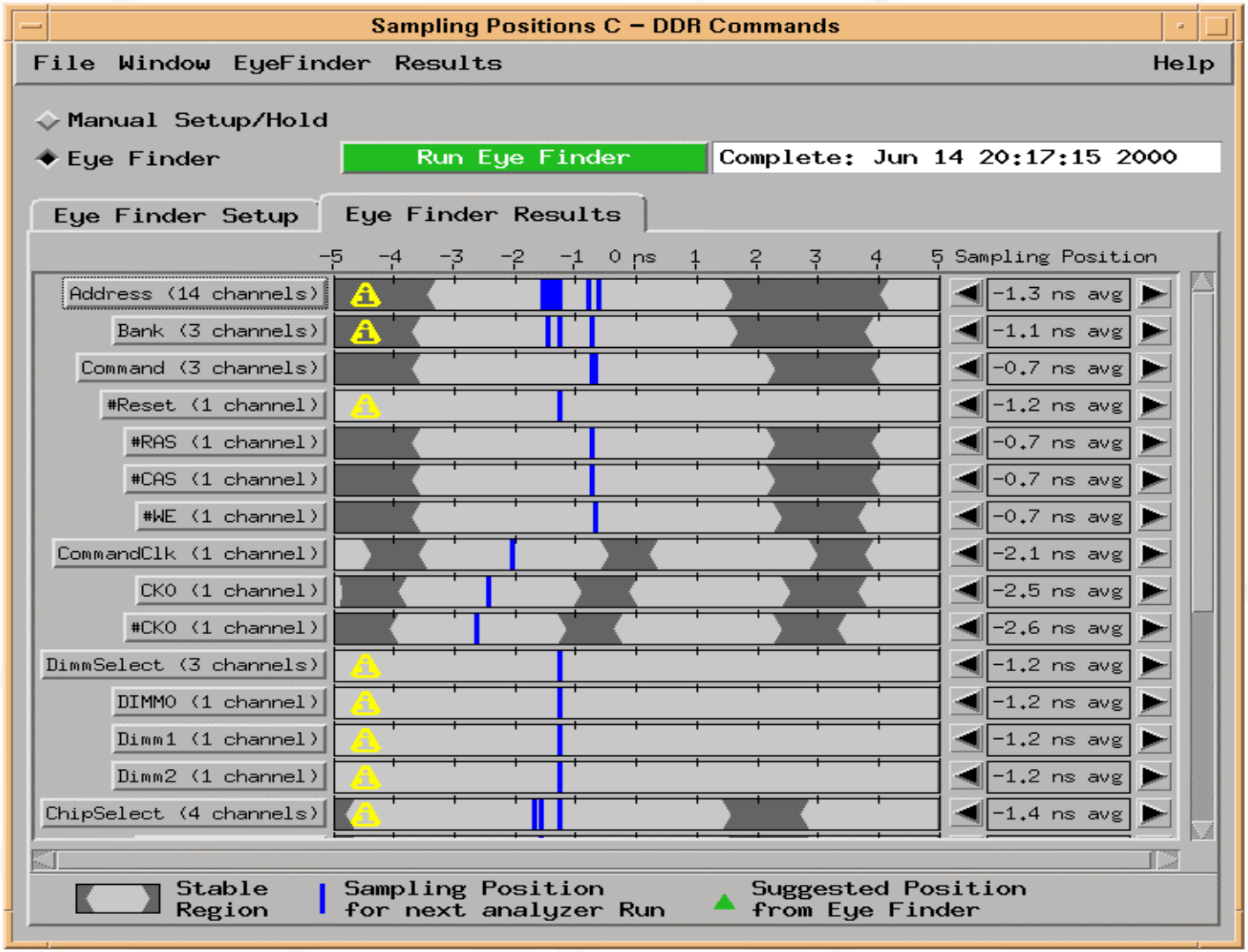


Adjustment is performed through probe calibration of delay lines.

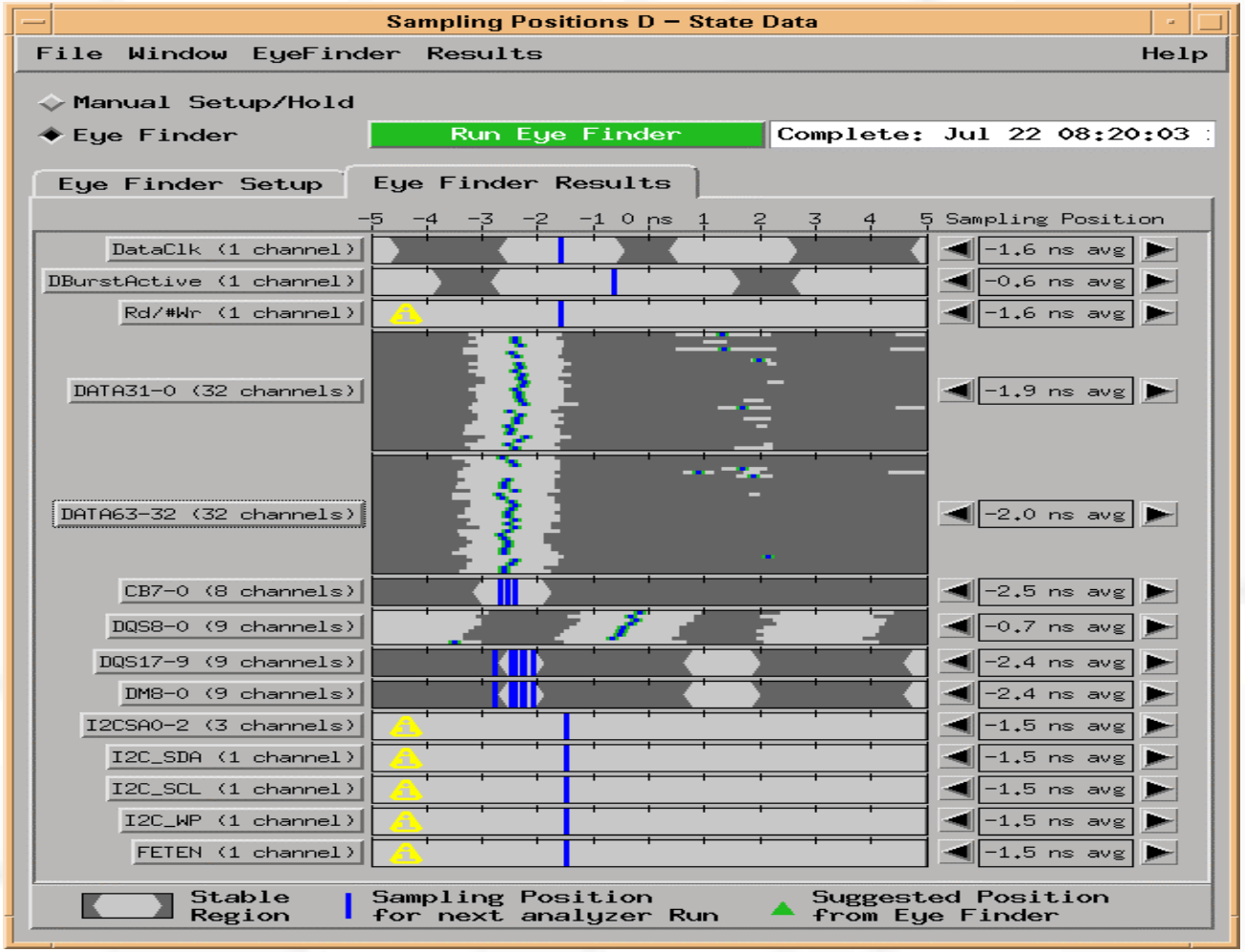
DDR Read Burst



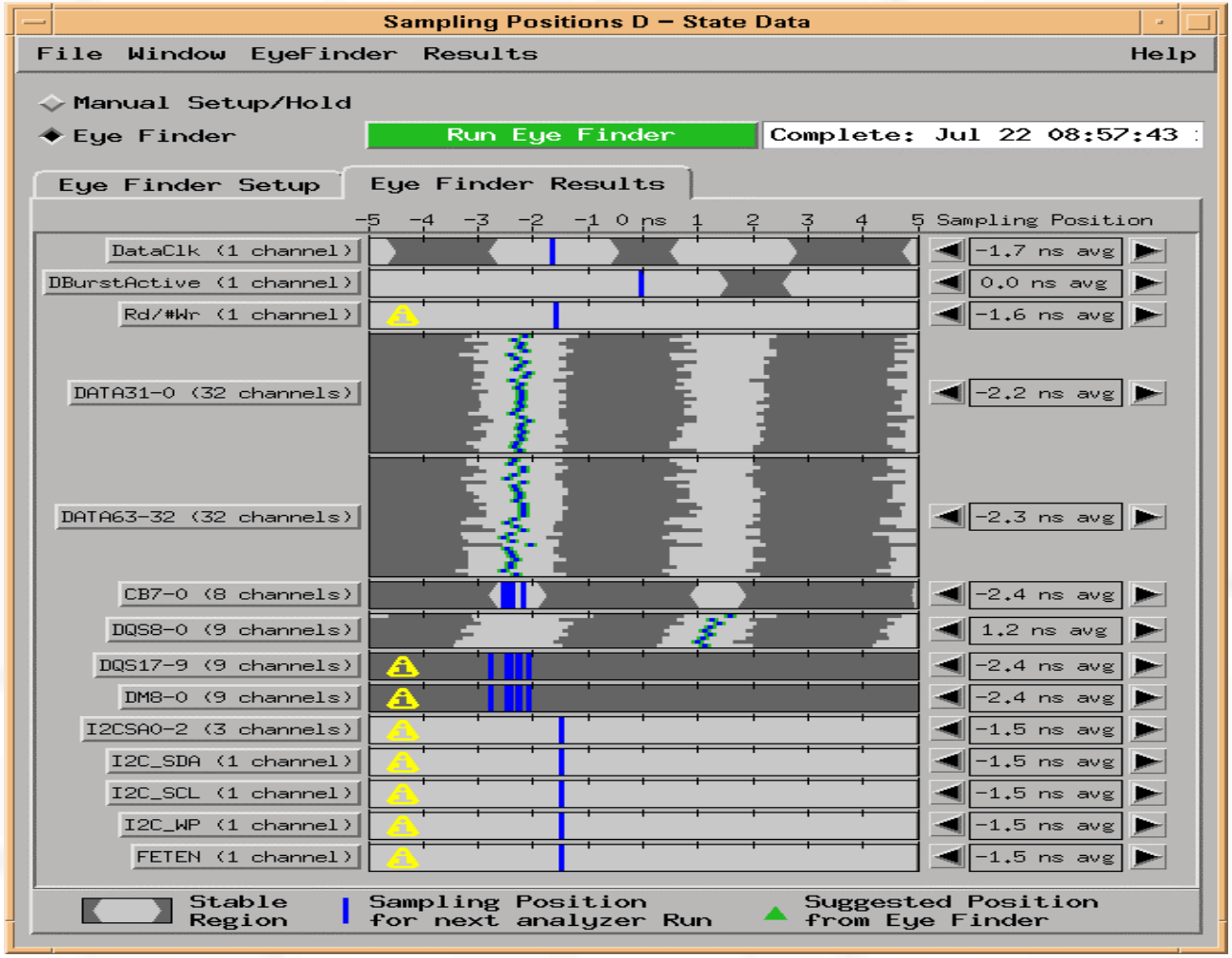
DDR Command Bus



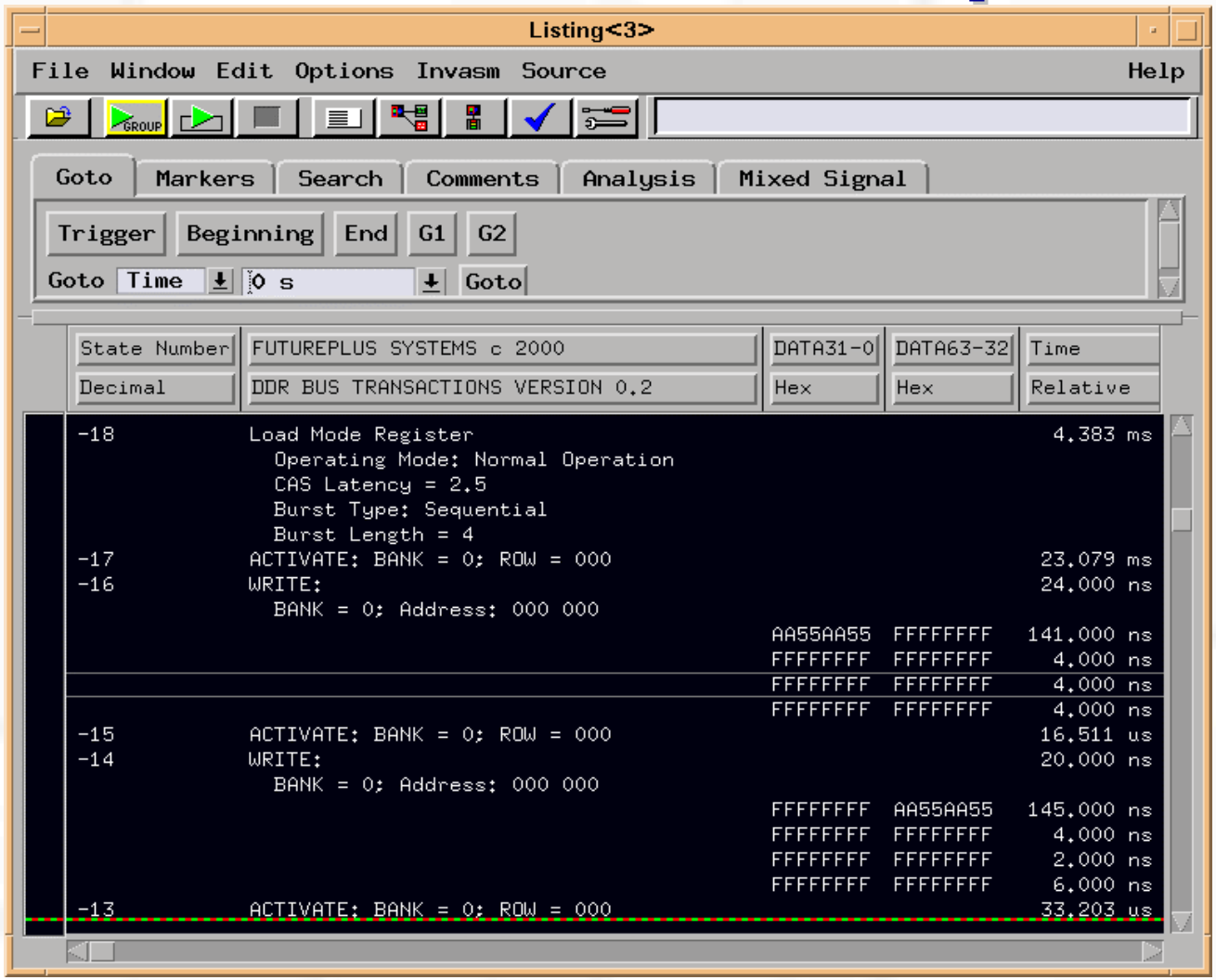
DDR Write Cycles



DDR Read Cycles



DDR Write Data Capture



Eye Finder - Insight at a Glance

- Is Eye size adequate for state analysis?
- Signal skews
- General timing/phase relationship of bus signals
- Possible signal integrity problems
- Sensitivity to temperature, voltage
- Duty cycle
- Jitter
- **All of the above are QUALITATIVE, not QUANTITATIVE**

DDR probe components

The following components ship with the FS2330 DDR Probe:

?FS2330 DDR DIMM Probe

?5V external power supply with IEC power cord (US 120V)

?Floppy disk(s) with inverse assembler and configurations.

?A kit containing several delay lines for use in calibrating the probe for optimal state data capture.

?Users Guide.

DDR Probe LA Configurations

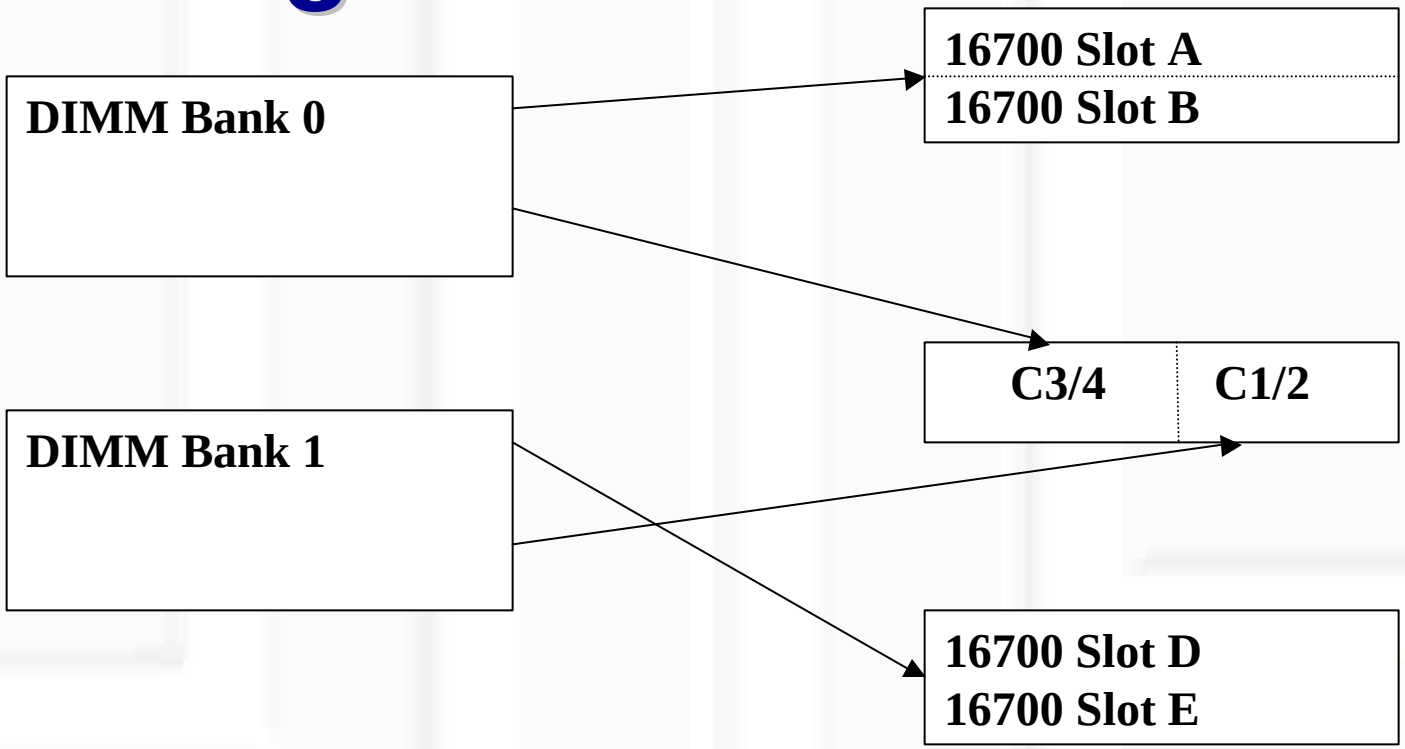
- **Timing mode - 2 cards configured as one module**

- **State mode - 3 cards**
  - **2 in turbo for data**
  - **1 in normal mode for command**

LA cards supported 16717/18/19A and 16750/51/52A

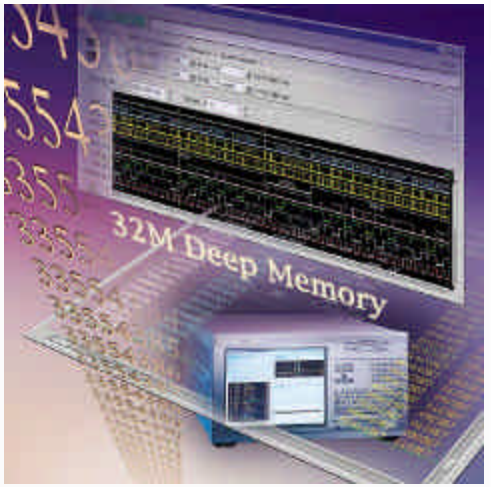
1675X Cards are recommended for the most accurate data capture.

DDR Probe LA Configurations continued



16750A, 16751A, 16752A 400 MHz Logic Analysis Modules

Shipping Since June 2000



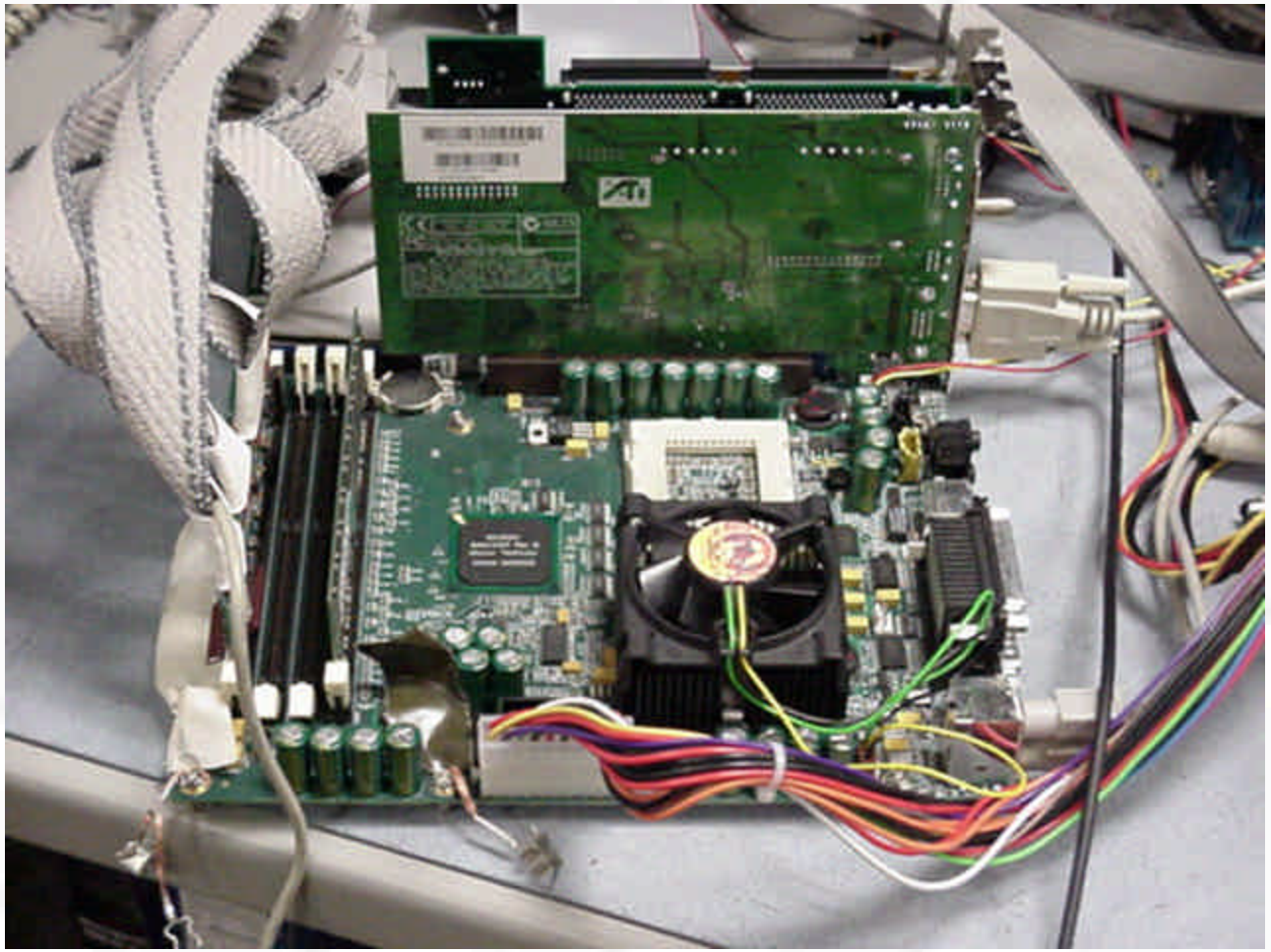
Key Specifications

- 200 MHz State
- 800/400 MHz Timing
- VisiTrigger
  - 16 Level Sequencer
  - 4 Way Branching
  - 2 Global Counters
  - 2 Global Timers
  - 4 Flags
  - 16+ Patterns
- 400 MHz "Turbo" State Triggering
  - 15 Level Sequencer
  - Sequence or Reset Branching
  - 8 Patterns
  - Flag Evaluation
- 2 GHz Timing Zoom, 16K
  - Simultaneous State and Timing Acquisition Through the Same Probe
- 4M, 16M, 32M Memory
- 68 Ch/Module
- 340 Ch/Group
- Setup & Hold

  2.5ns su/hd window
  adj +/- 4.5ns @ .1ns
  1.25ns su/hd window with Eye Finder
- Inputs:

  R=100Kohm, Tip C=1.5pF
  500mV pk-pk

DDR Probe Validation Setup



FS2330 DDR Probe Fits In Standard DIMM Slot